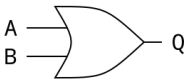
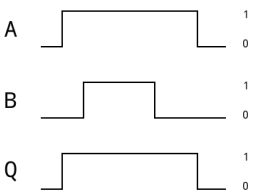
Introduction to Cycle-Accurate Verilog Simulation with Verilator

Graham Markall
(Compiler Engineer)

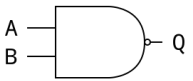
Verilog and Verilator

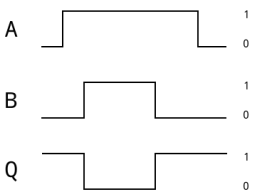
OR gate



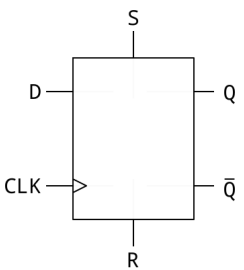


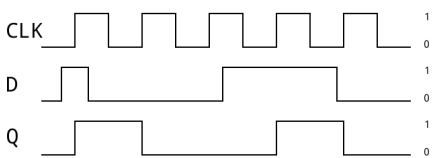
NAND gate





D flip-flop





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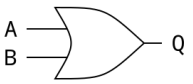
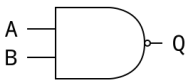
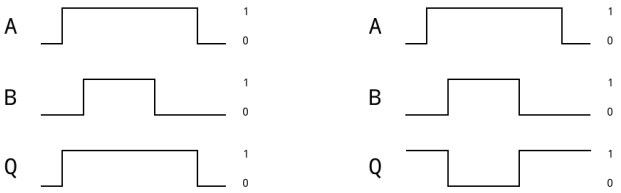
Verilog and Verilator

OR gate



NAND gate





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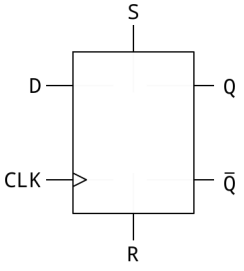

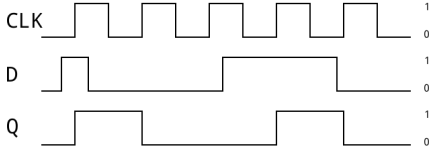


```
module toplevel(clock,
                reset);
  input clock;
  input reset;
  reg flop1;
  reg flop2;
  always @ (posedge clock)
    if (reset)
      begin
        flop1 <= 0;
        flop2 <= 1;
      end
    else
      begin
        flop1 <= flop2;
        flop2 <= flop1;
      end
endmodule
```

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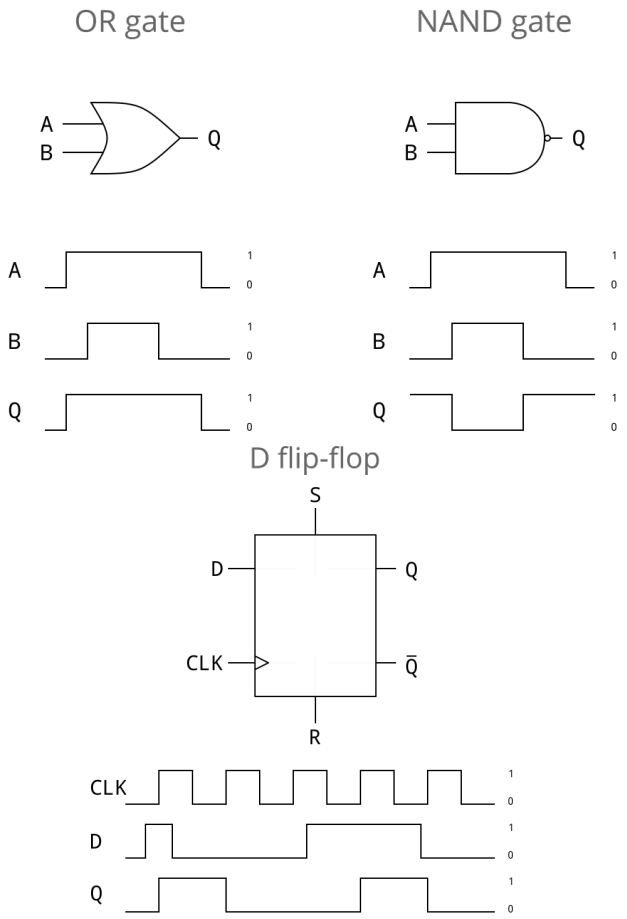
Verilog and Verilator

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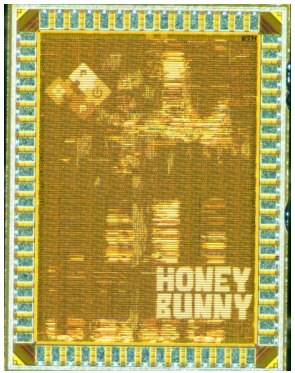

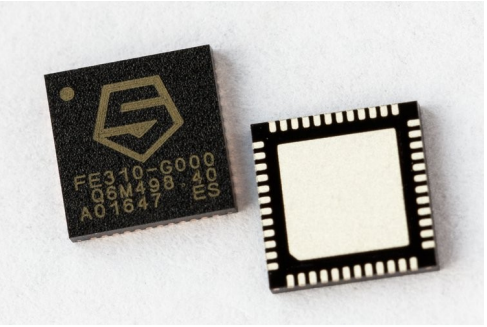

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My background (Embecosm)

Compiler Tool Chain Development

Embecosm are able to provide new and upgraded ports of binutils, GCC, GDB, GNU libraries, LLVM, LLDB, LLVM utilities and LLVM libraries, whether for the smallest deeply embedded processor, or the largest supercomputer cluster.

Hardware Modeling

Embecosm has extensive experience in all aspects of software modeling of hardware, from the creation of high-level transaction level models (TLM) through to fully cycle accurate simulations.

Open Source Tool Support

Embecosm provide a low risk route to adopting open source technology through tailored support packages for compiler toolchain ports and a wide range of open source EDA tools.

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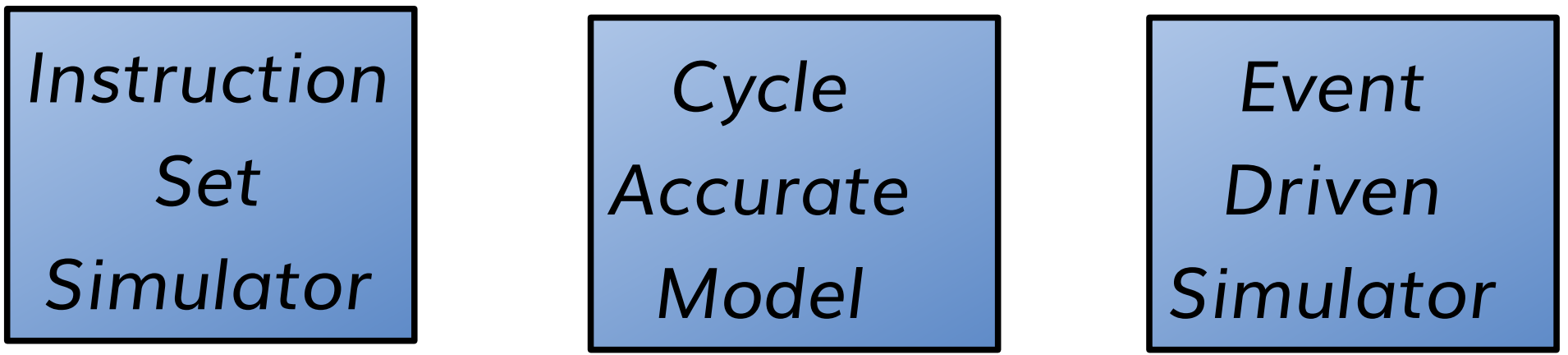
Outline

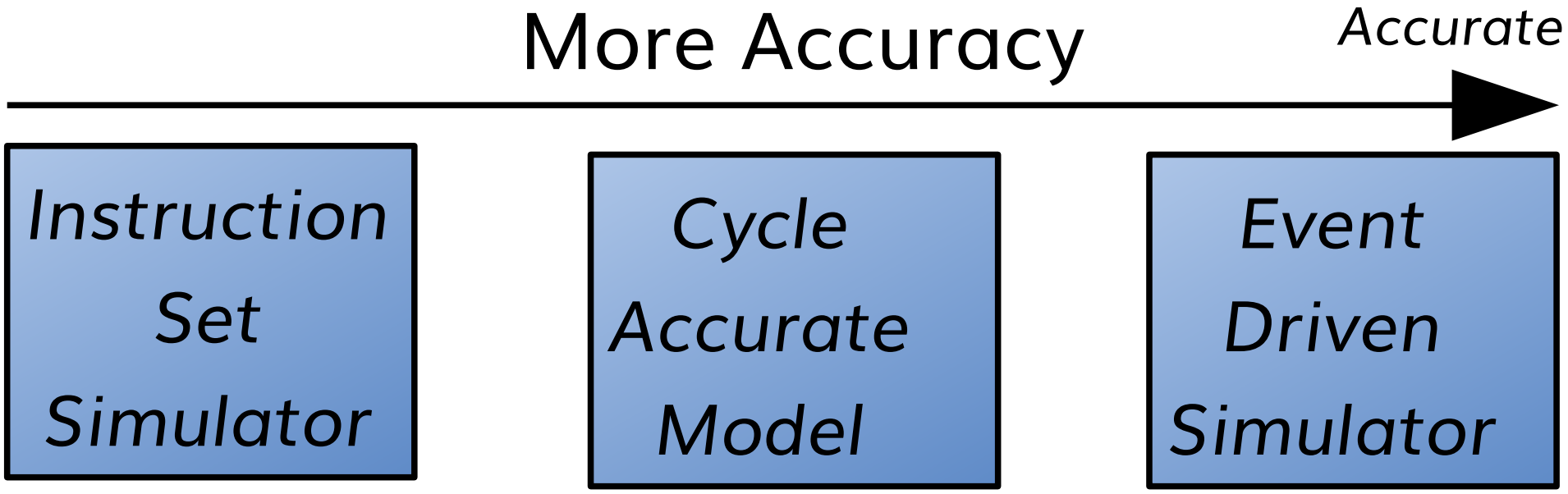
- Verilog refresher / quick primer
- Simulation approaches
- Using Verilator
- Visualising behaviour with trace files
- Workshop tomorrow

Verilog refresher / quick primer

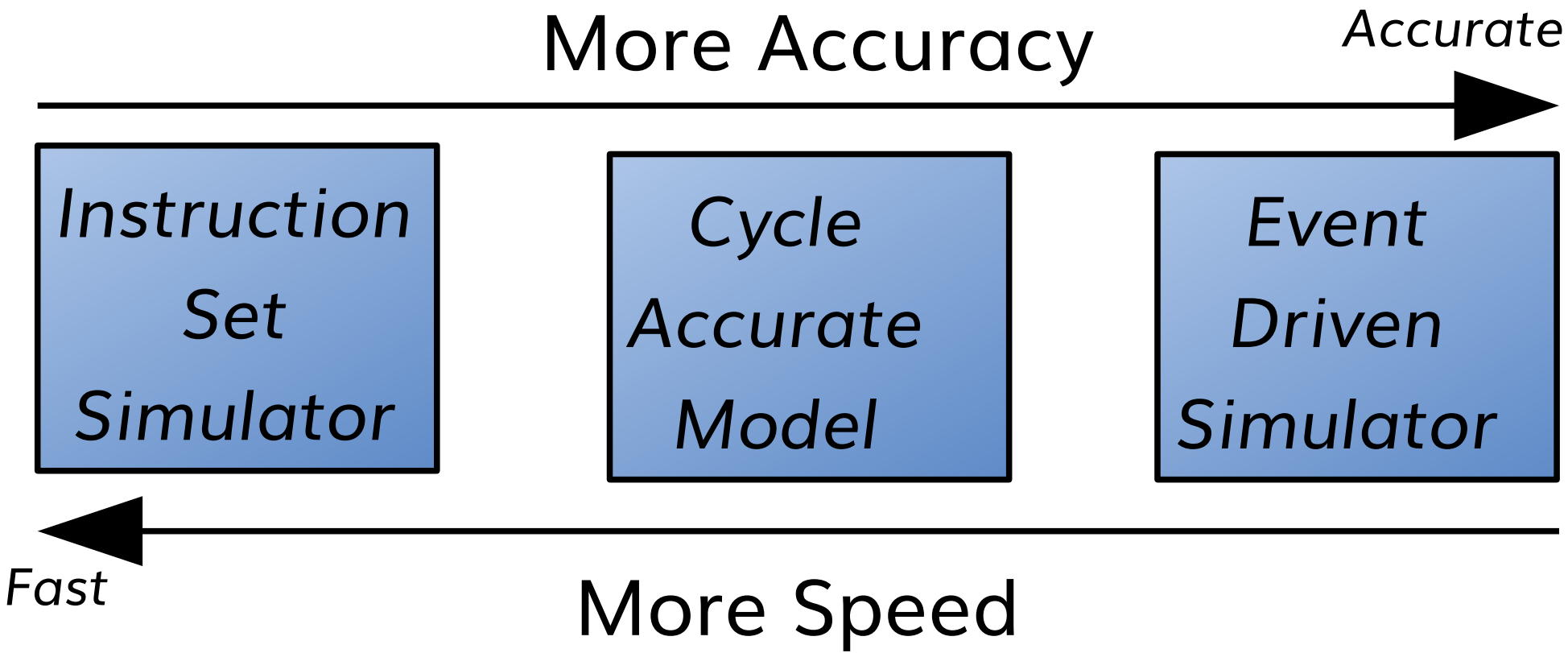
Simulation approaches (CPUs)



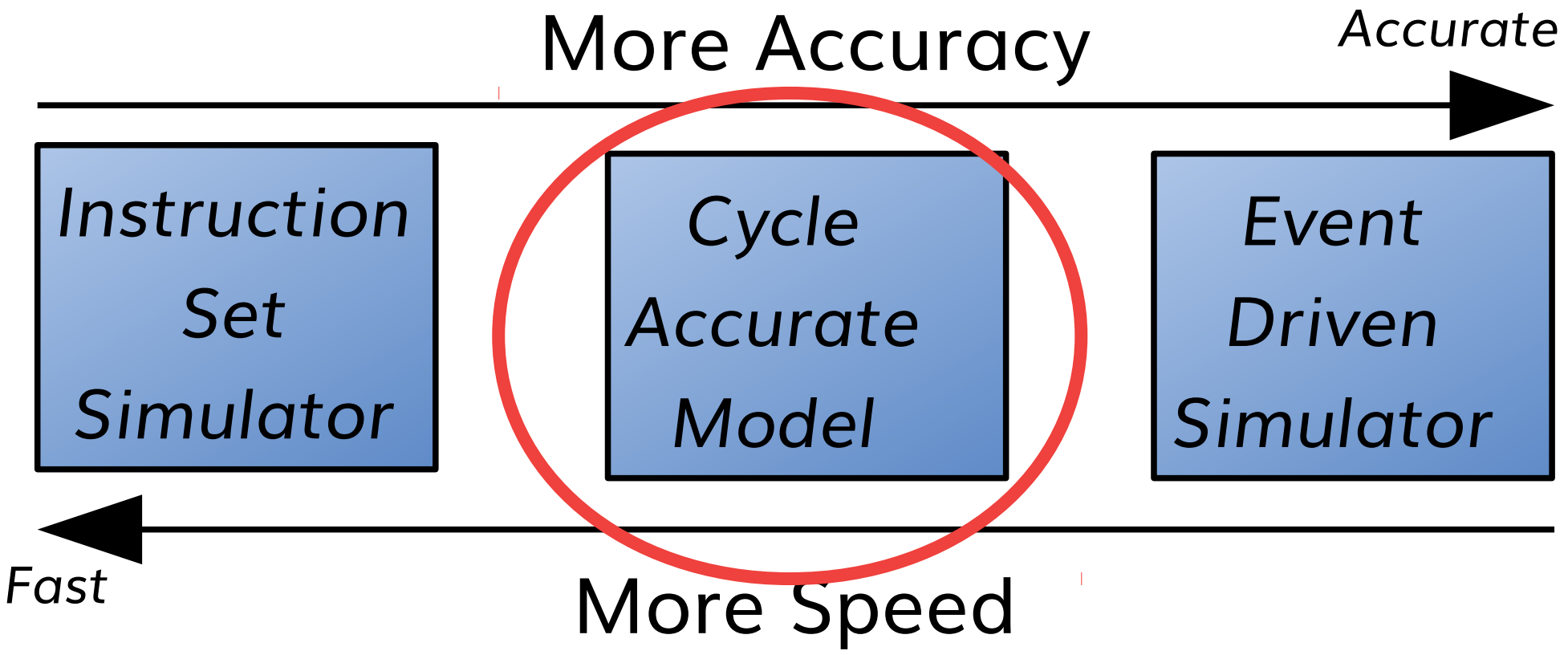
Simulation approaches



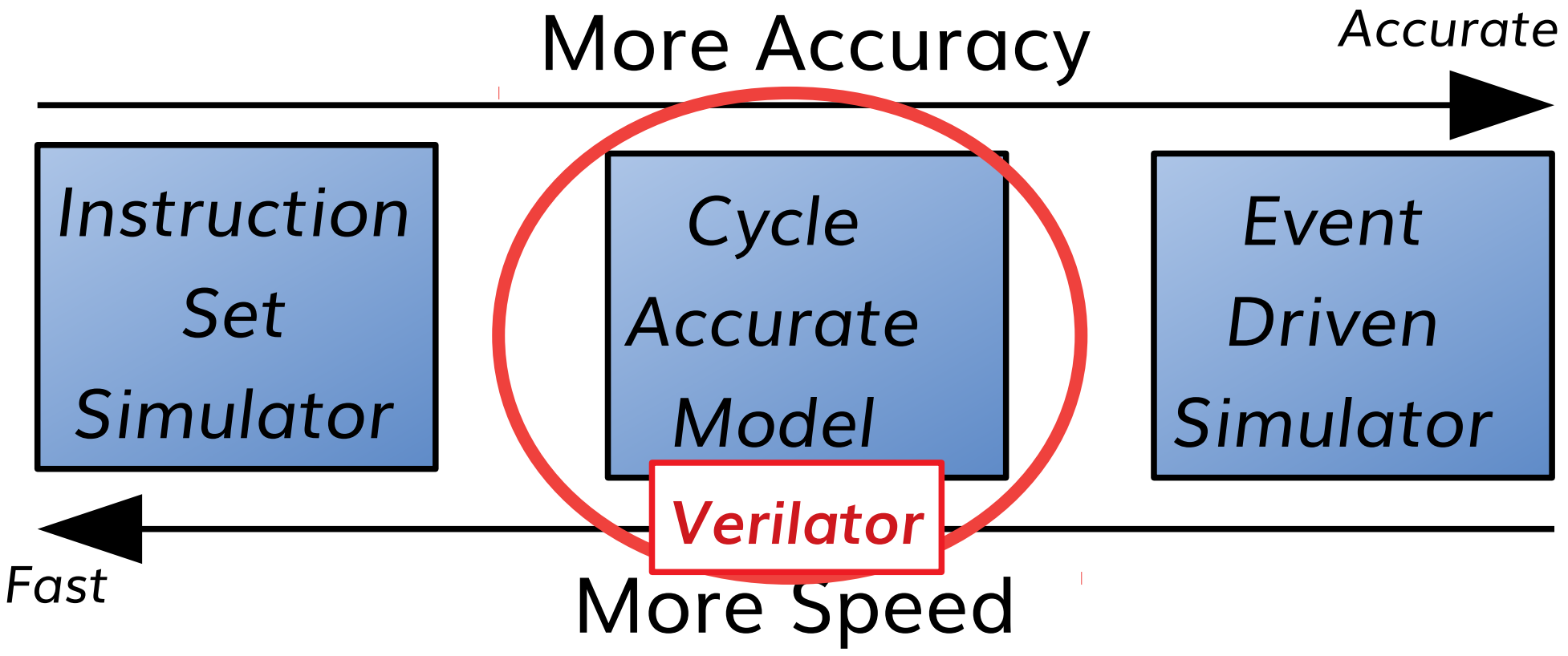
Simulation approaches



Simulation approaches



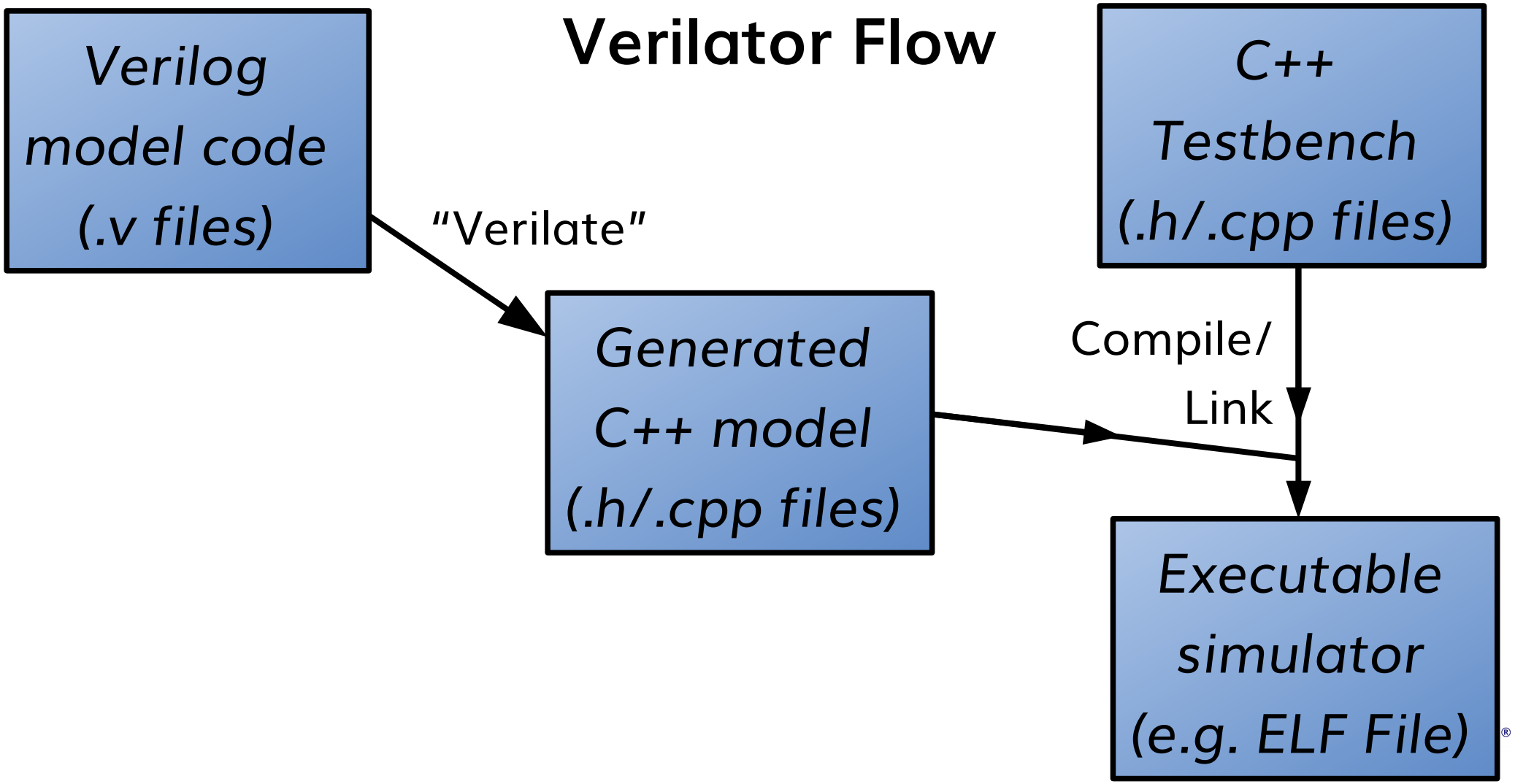
Simulation approaches



About Verilator

- Verilog → Cycle-accurate model in C++ or SystemC
- Free and open source, Veripool project
- Primary Author: Wilson Snyder
- Widely used in industry and academia:
  - NXP, ARM, CSR, Broadcom, Raytheon, Infineon, Imperial College, Embecosm (Wikipedia)

Verilator Flow



Switch back to Verilog slides

Workshop tomorrow:

Open Source RISC-V Core Quickstart

Basic Verilog / Verilator Counter

PicoRV32

RI5CY

Ariane

Graham Markall
(Compiler Engineer)